

Microprocessor & Interfacing
Lecture 22
8255
Programmable Peripheral Interface--1



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Introduction



- Peripheral interface are the intermediate devices which is used to communicate between the two devices for example if we connect computer and printer then these two device can not work here we required at least one device that can connect these two devices it could be USART or 8255 programmable peripheral interface.

PPI 8255



- Features:
 - It is a programmable device.
 - It has 24 I/O programmable pins like PA, PB, PC (3-8 pins).
 - T T L compatible.
 - Improved dc driving capability

Pin Diagram 8255



PA3	1		40	PA4
PA2	2		39	PA5
PA1	3		38	PA6
PA0	4		37	PA7
\overline{RD}	5		36	\overline{WR}
\overline{CS}	6		35	RESET
gnd	7		34	D0
A1	8		33	D1
A0	9		32	D2
PC7	10	8255	31	D3
PC6	11	PPI	30	D4
PC5	12		29	D5
PC4	13		28	D6
PC0	14		27	D7
PC1	15		26	Vcc
PC2	16		25	PB7
PC3	17		24	PB6
PB0	18		23	PB5
PB1	19		22	PB4
PB2	20		21	PB3

Pin Description



- Data bus(D0-D7):These are 8-bit bi-directional buses, connected to 8085 data bus for transferring data.
- CS': This is Active Low signal. When it is low, then data is transfer from 8085.
- Read': This is Active Low signal, when it is Low read operation will be start.
- Write': This is Active Low signal, when it is Low Write operation will be start.
- RESET: This is used to reset the device. That means clear control registers.

Cont..



- Address (A0-A1): This is used to select the ports.

A1	A0	Select
0	0	PA
0	1	PB
1	0	PC
1	1	Control reg.

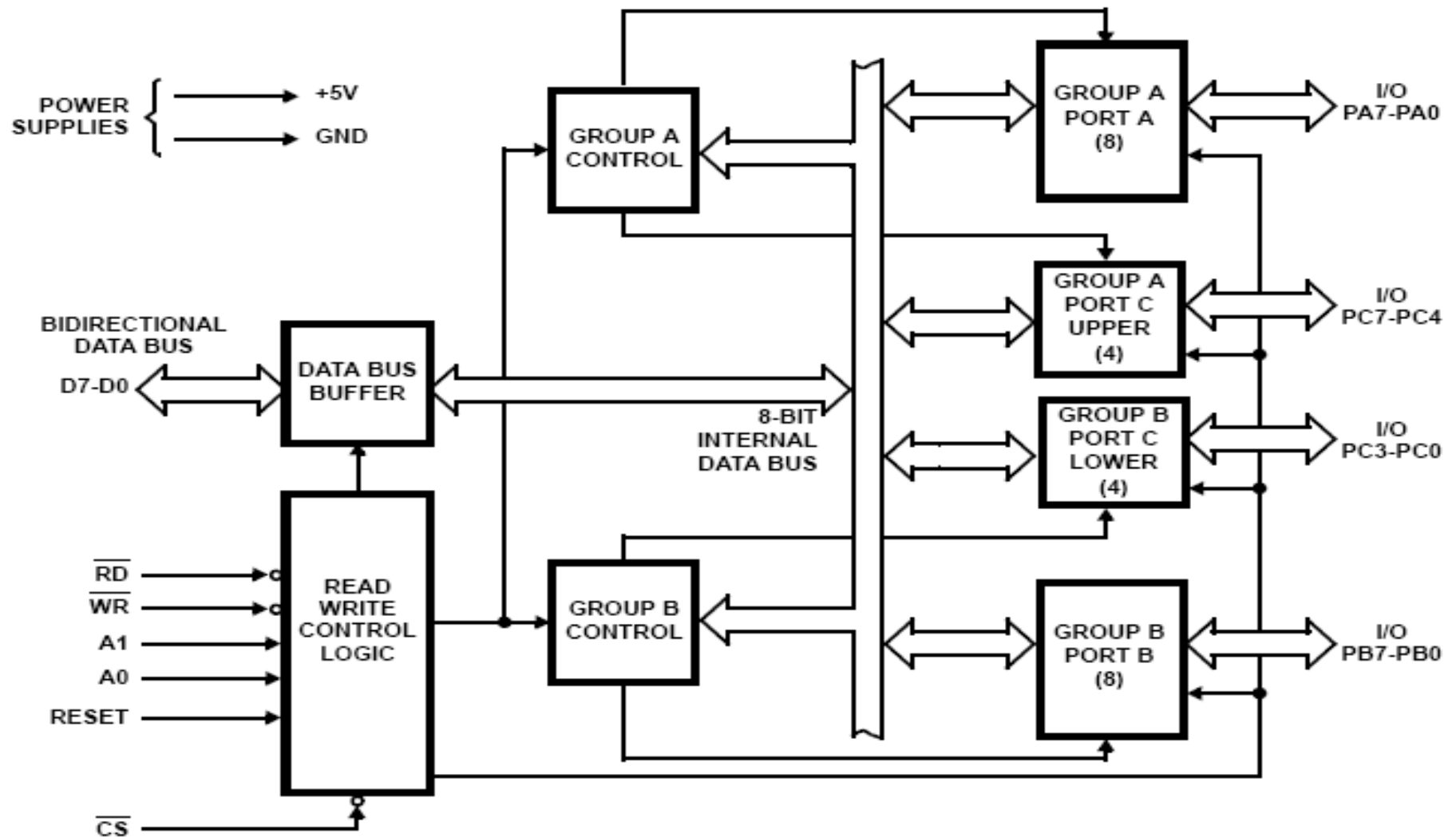
Cont..



- PA0-PA7: It is the 8-bit bi-directional I/O pins used to send the data to peripheral or to receive the data from peripheral.
- PB0-PB7: Similar to PA
- PC0-PC7: This is also 8-bit bidirectional I/O pins. These lines are divided into two groups.
 - 1. PC0 to PC3 (Lower Groups)
 - 2. PC4 to PC7 (Higher Groups)

These two groups work separately using 4 data.

Block Diagram



Data Bus Buffer



- It is a 8-bit bidirectional Data bus.
- Used to interface between 8255 data bus with system bus.
- The internal data bus and Outer pins D0-D7 pins are connected in internally.
- The direction of data buffer is decided by Read/Control Logic.

Read/Write Control Logic



- This is getting the input signals from control bus and Address bus
- Control signal are RD' and WR' .
- Address signals are $A0$, $A1$, and CS' .
- 8255 operation is enabled or disabled by CS' .